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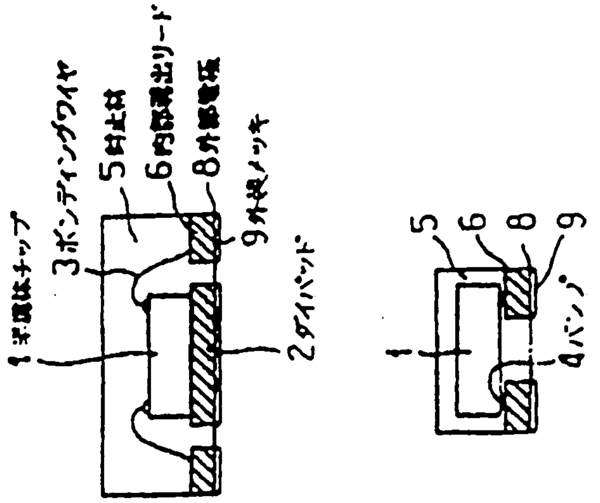
★SONY U11 93-202142/25 ★JP05129473-A

Mould package flat-face mounting type semiconductor device - exposes bottom surfaces of die pad and inner leads of bottom surface of mould package semiconductor device to be directly connected to circuit pattern of PCB NoAbstract

SONY CORP 91.11.06 91JP-289882
(93.05.25) *H01L 23/28, 23/12, 23/28, 23/50*
(6pp Dwg.No.1/13) U11-D01A3 U11-D03A9
N93-155203



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(22)Date of filing : 06.11.1991
(71)Applicant : SONY CORP
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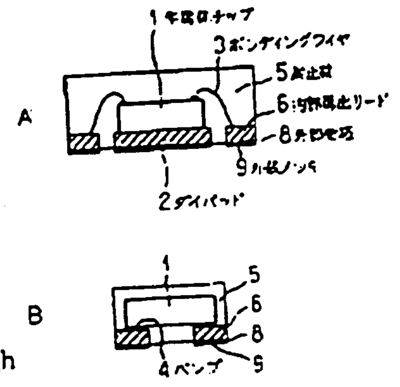
(54) RESIN-SEALED SURFACE-MOUNTING SEMICONDUCTOR DEVICE



(57)Abstract:
PURPOSE: To reduce the size and thickness of the title semiconductor device while a mechanism which prevents the deformation of external electrodes or fluctuation of the electrodes at the machining time is secured by using the rear sections of inner leads connected to internal wiring as external electrodes at the time of directly mounting the semiconductor device.
CONSTITUTION: A semiconductor chip 1 is placed on the die pad 2 of a lead frame. After electrically connecting the chip 1 to inner leads 6, the rear of which become external electrodes 8, through bonding wires 3, the upper part is sealed with a resin. Similarly, the chip 1 is electrically connected to the leads through bumps 4. In other words, the rear of the electrically connected inner leads 6 are used as the electrical connecting sections 8 of the semiconductor device to the outside. Therefore, the size of the semiconductor device can be reduced to nearly the same size as that of the chip 1. In addition, the thickness of the semiconductor device can also be reduced.

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CLAIMS

[Claim(s)]

[Claim 1] The resin-seal surface mount type semiconductor device with which the rear-face section of the internal derivation lead to which the aforementioned internal wiring is connected is characterized by the external electrode and bird clapper at the time of mounting a direct semiconductor device in the resin-seal surface mount type semiconductor device which carries a semiconductor device, wires an internal derivation lead in the electrode on the front face of an element, and comes to carry out the resin seal of the wiring section and the aforementioned semiconductor device section.

[Claim 2] The resin-seal surface mount type semiconductor device according to claim 1 characterized by the rear face of a semiconductor device being exposed to the outside of a semiconductor device through resin material other than a direct or closure resin.

[Claim 3] The resin-seal surface mount type semiconductor device according to claim 1 characterized by forming more highly one step than the field of an external electrode the field through the rear-face section of a semiconductor device, or resin material other than a closure resin.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] This invention relates to the surface mount type semiconductor device by which the resin seal was carried out.

[0002]

[Description of the Prior Art] It connects electrically to the interior derivation lead 6 of direct by the connection electrode called bump 4 as it connects electrically to the internal derivation lead 6 by the bonding wire 3 as a semiconductor chip 1 is carried in the die pad 2 of the leadframe made with the metal (0.1-0.3mm of board thickness [For example, being 42%nickel/Fe alloy.]) as a former and surface mount type semiconductor device shown to drawing 10 in the cross section of the example and it is shown in drawing 10 A, or shown in drawing 10 B. And after closing these with the sealing agents 5, such as an epoxy resin, the external derivation lead 7 and the external electrode 8 are bent and formed in a necessary configuration.

[0003] And as shown to drawing 11 A in a side elevation, as shown in a soldering paste 13 or drawing 11 B, adhesives 14 are applied to the pattern of a substrate 12 at the substrate 12, alignment of the surface mount type semiconductor device is carried out to this, and it is put on it. When a soldering paste 13 is used like drawing 11 A, this substrate 12 is heated by hot blast or infrared radiation, and is soldered. On the other hand, when adhesives 14 are used like drawing 11 B, it solders by being immersed in a solder tub.

[0004] However, the surface mount type semiconductor device mentioned above Since bending of the external derivation lead 7 and the external electrode 8 is carried out on the outside of the sealing agent 5 shown in drawing 10 A and B, According to the force from the variation of this process tolerance, and the outside after fabrication, as shown in the perspective diagram of drawing 12 A As shown in the variation of the position of the height direction of the inferior surface of tongue of the external electrode 8 to the base of the sealing agent 5 of a semiconductor device, and the plan of drawing 12 B, it is easy to produce deformation of the external derivation lead 7 to a longitudinal direction and the external electrode 8. These become a cause and a suitable surface mount becomes impossible the time of the above-mentioned substrate mounting. Or the technical problem of it becoming impossible to flow electrically occurred.

[0005] Then, in order to cancel this technical problem, like the semiconductor device currently indicated by JP,3-3354,A shown in drawing 13 , in the external electrode 8, it is the same field as the base of a sealing agent 5, and the configuration which drew in parallel with the base is proposed.

[0006]

[Problem(s) to be Solved by the Invention] by the way, it miniaturizes and electronic equipment thin-shape-izes in recent years -- having -- ****** -- the semiconductor device used is also required as achieving a miniaturization and thin shape-ization as much as possible, and it has a size of the semiconductor chip by which the size of a sealing agent is carried in the interior closely now, and the thin shape semiconductor device 1.0mm or less has been put in practical use also for thickness However, in such small and the thin shape semiconductor device, the technical problem that a size, and about [becoming large far from a semiconductor chip size] and thickness will become thick occurred in a configuration which is indicated by JP,3-3354,A shown in above-mentioned drawing 13 . while this invention maintains the mechanism in which deformation of an external electrode or the variation at the time of processing is prevented -- moreover -- a miniaturization -- a thin shape -- it aims at offering the resin-seal surface mount type semiconductor device [-izing / a semiconductor device]

[0007]

[Means for Solving the Problem] In order to solve a technical problem which was described previously, this invention used as the electrical installation portion, i.e., external electrode, with the exterior of a semiconductor device the rear face of an internal derivation lead electrically connected with an internal derivation lead by a semiconductor chip, a bonding wire, or the bump using the leadframe which has a die pad in the same flat surface.

[0008]

[Function] Therefore, since the resin-seal surface mount type semiconductor device of this invention used as the electrical installation portion, i.e., external electrode, with the exterior of a semiconductor device the rear face of an internal derivation lead electrically connected with an internal derivation lead by a semiconductor chip, a bonding wire, or the bump using the leadframe which has a die pad in the same flat surface, it can make the size of a semiconductor device small to the almost same size as the size of a semiconductor chip. Moreover, thickness of a semiconductor device can be made thin.

[0009]

[Example] Hereafter, the resin-seal surface mount type semiconductor device of the example of this invention is explained in full detail with a drawing. The cross section of the 1st example is shown in drawing 1 . First, drawing 1 A lays a semiconductor chip 1 in the die pad 2 of a leadframe with a thickness of 0.1-0.3mm, connects electrically the internal derivation lead 6 with which a semiconductor chip 1 and a rear face serve as the external electrode 8 by the bonding wire 3, and has structure which carried out the resin seal of the upper part. Drawing 1 B shows the example with which it is made to connect electrically a semiconductor chip 1 and the internal derivation lead 6 by the bump 4 similarly. Although there is an advantage that the electrical installation by the bump 4 can make still smaller the size of the structure top sealing agent 5 from the electrical installation method by the bonding wire 3, since the thickness of the resin of the inferior surface of tongue of a semiconductor chip 1 also becomes thin so that the board thickness of a leadframe is thin, it becomes easy to generate faults, such as a void at the time of a resin seal (foam).

[0010] The creation method of the semiconductor device of the 1st example is briefly explained using the cross section of drawing 2 and drawing 3 . First, the cross section of drawing 2 explains the 1st creation method. As shown in drawing 2 A, the internal derivation lead 6 connects electrically the semiconductor chip 1 and the internal derivation lead 6 with a die pad 2 by the bonding wire 3 after laying a semiconductor chip 1 using the leadframe in a coplanar by the same method as usual. Next, the sealing agents 5, such as an epoxy resin, are used and closed. And it is made the configuration which shaves off the rear-face resin section of a semiconductor device, and is shown in drawing 2 B. Then, in order to improve the soldering nature at the time of performing substrate mounting, it becomes like drawing 2 C by giving sheathing plating 9 of solder etc. to the portion which the external electrode 8 exposed. In this way, if the excessive portion of the outside of the external derivation lead 7 of the semiconductor device which was able to be done is cut using metal mold etc., the semiconductor device of this example shown in drawing 2 D will be obtained. Below, the cross section of drawing 3 explains the 2nd creation method. After laying a semiconductor chip 1 and connecting electrically like the 1st creation method, it becomes the configuration shown in drawing 3 A by performing a resin seal with the metal mold which has a cavity (********) only in the upper surface. Then, the semiconductor device of this example shown in drawing 3 B is obtained like the 1st creation method by performing cutting of the sheathing plating 9 and the external derivation lead 7. Although pretreatment called deburring ** by high-pressure water etc. is needed before giving sheathing plating 9 since the barricade at the time of a resin seal etc. may have adhered to the portion which is going to give sheathing plating 9 in the case of this creation method, the work of shaving off a stiff closure resin like the 1st creation method is omissible.

[0011] The cross section of the 2nd example is shown in drawing 4 . Although not structurally divided ********* with the 1st three operations, the thickness of the die pad 2 which lays a semiconductor chip, and the external electrode 8 consists of very thin (about 10-30 micrometers) conductors, such as copper foil. The structure of this example becomes possible [making thin hundreds of micrometers thickness of a semiconductor device compared with the 1st example]. Moreover, since the rear face of a semiconductor chip 1 has structure exposed outside through direct or a metal part, there is also an advantage of being easy to miss the heat generated from a semiconductor device, after substrate mounting at the time of use. The creation method of the semiconductor device of this 2nd example is briefly explained using the cross section of drawing 5 . Although a leadframe is used in the 1st example mentioned above Laminate thin conductors, such as copper foil, on the films 10, such as a polyimide which the hole opened partially as shown in drawing 5 A by this example, and a die pad 2, the internal derivation lead 6, and the external wiring 11 are formed. this conductor -- a semiconductor chip 1 is laid in the with **** film 10 like the above-mentioned method, and it connects with it electrically, and if a resin seal and sheathing plating 9 are given, it will become the structure which shows the cross section in drawing 5 B Furthermore, if a film 10 is exfoliated giving heating etc., it will become the structure of this example as shown in drawing 5 C. In addition, in case a film 10 is exfoliated on the outside of the external electrode 8 used for this example, it is good to make thin beforehand external wiring 11 connected to an external electrode as shown in the plan of drawing 5 D so that a portion with an excessive conductor may cut simultaneously.

[0012] The cross section of the 3rd example is shown in drawing 6 . In the 3rd example, it has the films 10, such as a polyimide, under the die pad 2 which lays a semiconductor chip 1. Although there are not an example mentioned above and a changing place out of it, since only the part of the thickness of the external electrode 8 has a film 10 in a high place to the height of the base of the external electrode 8 used as a part for the connection at the time of substrate mounting in the case of this example, there is an advantage that there is a cleaning effect of the flux after substrate mounting. Moreover, since there is no portion electrically connected with the rear face of a semiconductor chip 1 in the center of a semiconductor device, there is also imitation or an advantage that there is nothing, about which short fault generated at the time of substrate mounting. In addition, although drawing where a die pad 2 exists has explained by this example, on the occasion of operation, it is not not necessarily the need. The creation method of the semiconductor device of the 3rd example is briefly explained using the cross section of drawing 7 . In the 3rd example, thin conductors, such as copper foil, are laminated on the films 10, such as a polyimide which the hole opened partially as shown in drawing 7 A, a die pad 2, the internal derivation lead 6, and the external wiring 11 are formed, and it becomes the structure which shows the cross section in it at drawing 7 B when a semiconductor chip 1 is laid in the film 10 to which this conductor was attached like the above-mentioned method, it connects with it electrically and a resin seal and sheathing plating 9 are given to Furthermore, if the film 10 of the semiconductor device circumference is exfoliated giving heating etc., it will become the structure of this example as shown in drawing 7 C. In addition, it is good to make thin beforehand external wiring 11 of the outside of the external electrode 8 like the 2nd example, so that it may be easy to cut in case a film 10 is exfoliated.

[0013] Furthermore, as the 4th and 5th examples, as a cross section is shown in drawing 8 , it is created more easily than the example which has also mentioned above the structure which has arranged the external electrode 8 doubly. In the case of the structure of this example, although the size of a semiconductor device becomes somewhat large from the above-mentioned example, since the interval of external electrode 8 comrades is made widely, there is an advantage of being hard to generate the bridge (inter-electrode short-circuit) by the solder at the time of substrate mounting.

[0014] Moreover, it sets in the 3rd example shown in the cross section of drawing 6 as the 6th example. Since the field which minded the rear-face section of a semiconductor chip 1 or resin material other than sealing agent 5 by removing the film 10 in the center section of the completed semiconductor device as shown in a cross section is made still more highly than the surface of tongue of the external electrode 8 There is an advantage that the cleaning effect at the time of foundation mounting which the 3rd example described by the way goes up more.

[0015]

[Effect of the Invention] Since the rear face of the node of an internal derivation lead was used as the external electrode of a semiconductor device, with the semiconductor device of this invention, the semiconductor device of the size near the size of a semiconductor chip can be offered, so that clearly from the above explanation. Moreover, the semiconductor device of the thickness around about 0.5mm can be offered also about thickness.

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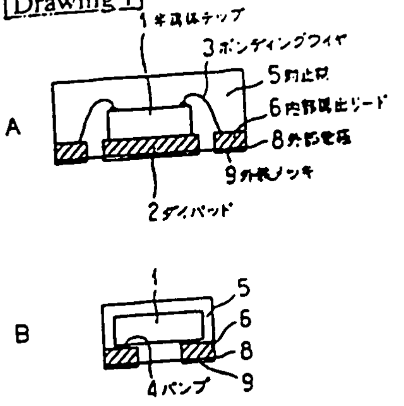
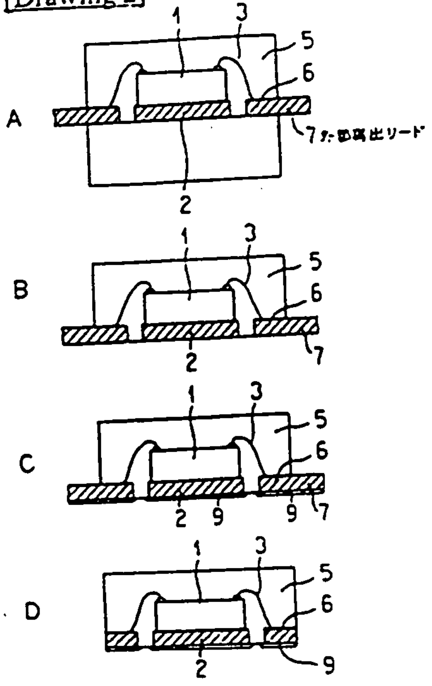
DRAWINGS

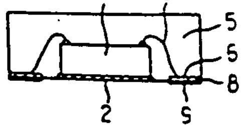
[Drawing 1]

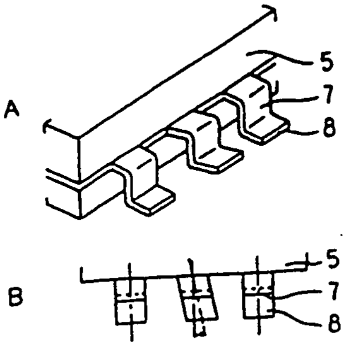


[Drawing 2]

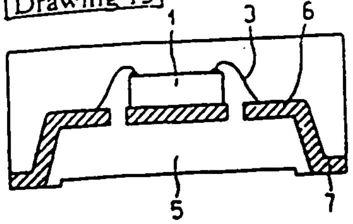


[Drawing 4]





[Drawing 13]



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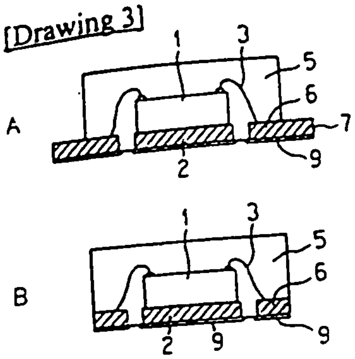
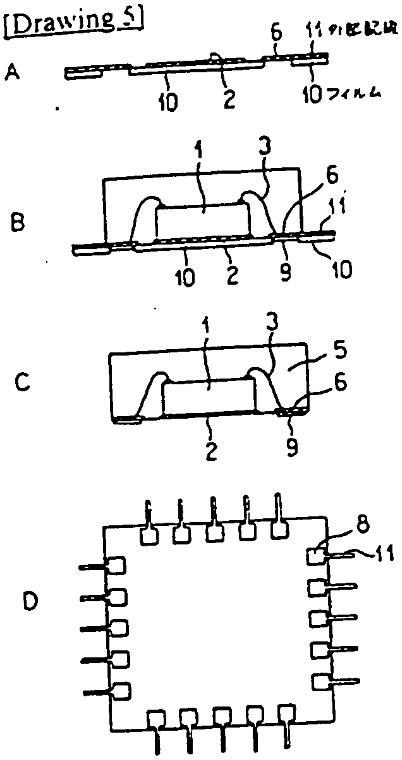
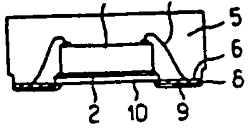
[Drawing 3]



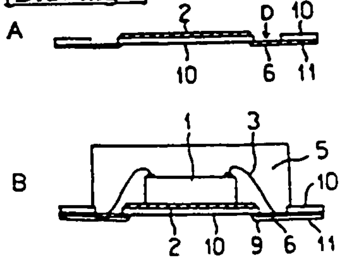
[Drawing 5]



[Drawing 6]



[Drawing 7]



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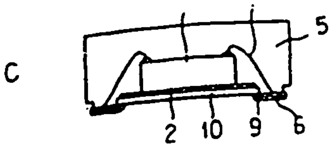
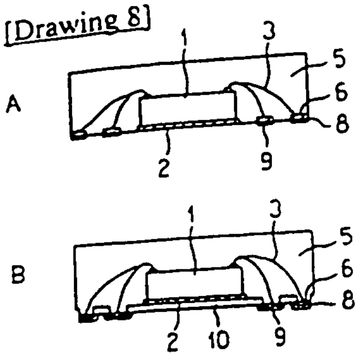
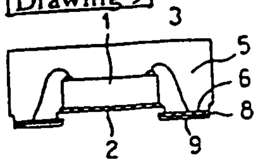


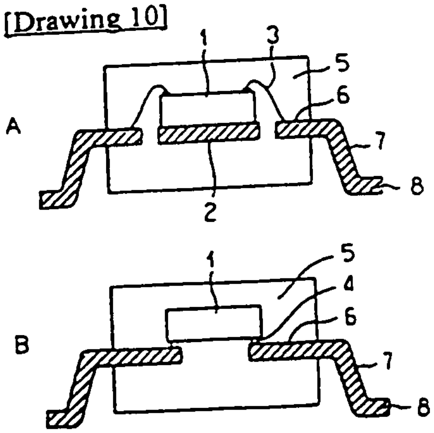
[Drawing 8]



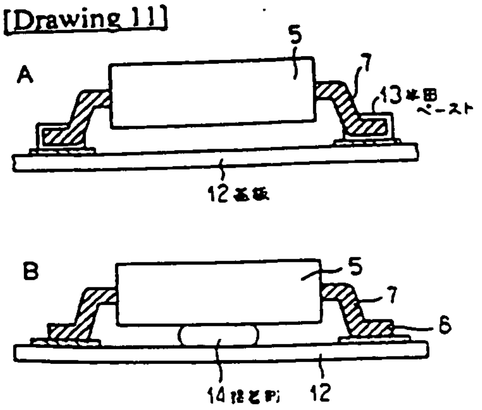
[Drawing 9]



[Drawing 10]



[Drawing 11]



[Drawing 12]

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23/28	A	8617－4M		
23/50	N	9272－4M		
		7352－4M	H01L　23／12	L

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(22)出願日　平成３年(1991)11月６日

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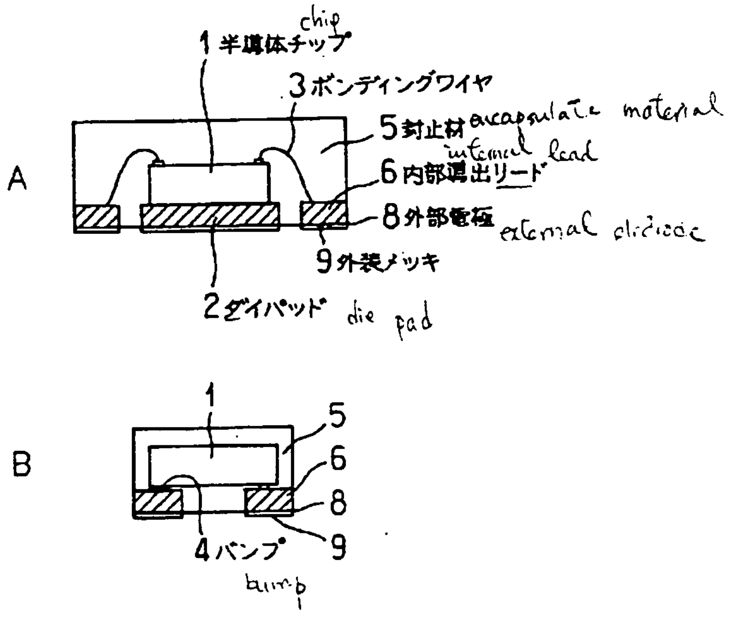
(54)【発明の名称】　**樹脂封止表面実装型半導体装置**

(57)【要約】

【目的】　小型化、薄型化可能な半導体装置を提供する。

【構成】　内部導出リード６とダイパッド２が同一平面にあるリードフレームを用い、半導体チップ１とボンディングワイヤ３あるいはバンプ４により電気的に接続されている内部導出リード６の裏面を、半導体装置の外部との電気的接続部分として機能する外部電極８とする。



【特許請求の範囲】

【請求項１】　半導体素子を搭載し、その素子表面の電極を内部導出リードに配線し、その配線部および前記半導体素子部を樹脂封止してなる樹脂封止表面実装型半導体装置において、
前記内部配線の接続される内部導出リードの裏面部が、直接半導体装置を実装する際の外部電極となることを特徴とする樹脂封止表面実装型半導体装置。

【請求項２】　半導体素子の裏面が直接あるいは封止樹脂以外の樹脂材料を介して、半導体装置の外側に露出していることを特徴とする請求項１記載の樹脂封止表面実装型半導体装置。

【請求項３】　半導体素子の裏面部あるいは封止樹脂以外の樹脂材料を介した面が、外部電極の面よりも一段高く形成されていることを特徴とする請求項１記載の樹脂封止表面実装型半導体装置。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】この発明は樹脂封止された表面実装型半導体装置に関するものである。

【０００２】

【従来の技術】従来、表面実装型半導体装置は図１０にその一例の断面図で示すように、金属（例えば、４２％Ｎｉ／Ｆｅ合金で、板厚０．１～０．３mm）でできたリードフレームのダイパッド２に半導体チップ１を搭載し、図１０Ａに示すように、ボンディングワイヤ３により内部導出リード６に電気的に接続するか、あるいは図１０Ｂに示すように、バンプ４と呼ばれる接続電極によって直接内部導出リード６に電気的に接続する。そして、これらをエポキシ樹脂などの封止材５で封止した後、外部導出リード７および外部電極８を所要の形状に曲げ形成している。

【０００３】そして、図１１Ａに側面図で示すように、基板１２のパターンに半田ペースト１３を、あるいは図１１Ｂに示すように、基板１２に接着剤１４を塗布しておき、これに表面実装型半導体装置を位置合わせして載せる。この基板１２を、図１１Ａのように半田ペースト１３を使用した場合には、熱風あるいは赤外線などにより加熱し半田付けする。一方、図１１Ｂのように接着剤１４を使用した場合には、半田槽に浸漬して半田付けを行う。

【０００４】しかしながら、前述した表面実装型半導体装置は、図１０Ａ、Ｂに示す封止材５の外側において、外部導出リード７および外部電極８を曲げ加工しているため、この加工精度のバラツキおよび成形後の外部からの力により、図１２Ａの斜視図に示すように、半導体装置の封止材５の底面に対する外部電極８の下面の高さ方向の位置のバラツキおよび図１２Ｂの平面図に示すように、横方向への外部導出リード７および外部電極８の変形が生じやすい。これらが原因となって前述の基板実装時、好適な表面実装ができなくなる。または、電気的に導通できなくなるという課題が発生した。

【０００５】そこで、この課題を解消するため、図１３に示した特開平３－３３５４号公報に開示されている半導体装置のように、外部電極８を封止材５の底面と同一面で、かつ底面と並行に導出した形状が提案されている。

【０００６】

【発明が解決しようとする課題】ところで、近年、電子機器が小型化、薄型化されるにしたっがって、使用される半導体装置もできるだけ小型化、薄型化をはかるように要求され、現在では封止材の大きさが内部に搭載されている半導体チップの大きさと近くなってきており、また、厚みも１．０mm以下の薄型半導体装置が実用化されてきている。しかし、このような小型、薄型半導体装置において、前述の図１３に示す特開平３－３３５４号公報に記載されているような形状では、大きさも半導体チップサイズよりはるかに大きくなってしまうばかりか、厚さも厚くなってしまうという課題が発生した。この発明は、外部電極の変形あるいは加工時のバラツキを防止する機構を保ちながら、しかも、小型化、薄型化可能な樹脂封止表面実装型半導体装置を提供することを目的とする。

【０００７】

【課題を解決するための手段】先に述べたような課題を解決するために、この発明は、内部導出リードとダイパッドが同一平面にあるリードフレームを用い、半導体チップとボンディングワイヤあるいはバンプにより電気的に接続される内部導出リードの裏面を、半導体装置の外部との電気的接続部分すなわち外部電極とした。

【０００８】

【作用】したがってこの発明の樹脂封止表面実装型半導体装置は、内部導出リードとダイパッドが同一平面にあるリードフレームを用い、半導体チップとボンディングワイヤあるいはバンプにより電気的に接続される内部導出リードの裏面を半導体装置の外部との電気的接続部分すなわち外部電極としたので、半導体装置の大きさを半導体チップの大きさとほぼ同じ大きさまで小さくすることができる。また、半導体装置の厚みを薄くすることができる。

【０００９】

【実施例】以下、この発明の実施例の樹脂封止表面実装型半導体装置を図面とともに詳述する。図1に第1の実施例の断面図を示す。まず、図１Ａは、厚さ０．１～０．３mmのリードフレームのダイパッド２に半導体チップ１を載置し、半導体チップ１と裏面が外部電極８となる内部導出リード６とをボンディングワイヤ３で電気的に接続させて、その上部を樹脂封止した構造となっている。図１Ｂは、同様に半導体チップ１と内部導出リード６とをバンプ４で電気的に接続をさせている例を示

す。ボンディングワイヤ3による電気的接続法よりバンプ4による電気的接続の方が、その構造上封止材5の大きさをさらに小さくできるという利点があるが、リードフレームの板厚が薄いほど半導体チップ1の下面の樹脂の厚みも薄くなるため、樹脂封止時のボイド（気泡）などの不具合が発生しやすくなる。

【0010】第1の実施例の半導体装置の作成方法を図2、図3の断面図を用いて簡単に説明する。まず、第1の作成方法を図2の断面図で説明する。図2Aに示すように、従来と同様の方法でダイパッド2と内部導出リード6が同一平面上にあるリードフレームを用い、半導体チップ1を載置後その半導体チップ1と内部導出リード6とをボンディングワイヤ3により電気的に接続を行う。つぎに、エポキシ樹脂などの封止材5を用いて封止する。そして、半導体装置の裏面樹脂部を削り取り図2Bに示す形状にする。その後、基板実装を行う際の半田付け性をよくするために、外部電極8の露出した部分に半田などの外装メッキ9を施すことにより図2Cのようになる。こうしてできた半導体装置の外部導出リード7の外側の余分な部分を金型などを用いて切断すると図2Dに示す本実施例の半導体装置が得られる。つぎに、第2の作成方法を図3の断面図で説明する。第1の作成方法と同様に、半導体チップ1を載置して電気的に接続した後、上面にのみキャビティ（堀り混み）のある金型で樹脂封止を行うことにより、図3Aに示す形状となる。この後、第1の作成方法と同様に、外装メッキ9および外部導出リード7の切断を行うことにより、図3Bに示す本実施例の半導体装置が得られる。この作成方法の場合、樹脂封止時のバリなどが外装メッキ9を施そうとしている部分に付着していることがあるため、外装メッキ9を施す前に高圧水などによるバリ取りという前処理が必要となるが、第1の作成方法のような硬い封止樹脂を削り取るという作業は省略できる。

【0011】図4に第2の実施例の断面図を示す。構造的には第1の実施3例とほとんど変わらないが、半導体チップを載置するダイパッド2および外部電極8の厚みが銅箔などの非常に薄い（約10～30μm）導体で構成されている。本実施例の構造は第1の実施例に比べ半導体装置の厚みを数百μmも薄くすることが可能となる。また、半導体チップ1の裏面が、直接あるいは金属部分を介して外部に露出している構造となっているので、基板実装後、使用時に半導体装置から発生する熱を逃がしやすいという利点もある。この第2の実施例の半導体装置の作成方法を図5の断面図を用いて簡単に説明する。前述した第1の実施例では、リードフレームを使用するが、本実施例では図5Aに示すような部分的に穴の開いたポリイミドなどのフィルム10に銅箔などの薄い導体をラミネートしてダイパッド2、内部導出リード6および外部配線11を形成し、この導体付いたフィルム10に、前述の方法と同様に半導体チップ1を載置して電気的に接続を行い、樹脂封止および外装メッキ9を施すと図5Bにその断面図を示す構造になる。さらに、加熱などを施しながらフィルム10を剥離すると図5Cに示すような本実施例の構造となる。なお、本実施例に用いられる外部電極8の外側に、フィルム10を剥離する際に導体の余分な部分が同時に切断してしまうように、図5Dの平面図に示したように外部電極に接続される外部配線11をあらかじめ細くしておくとよい。

【0012】図6に第3の実施例の断面図を示す。第3の実施例では半導体チップ1を載置するダイパッド2の下にポリイミドなどのフィルム10を有する。その外には前述してきた実施例と変わるところはないが、本実施例の場合、基板実装時の接続部分となる外部電極8の底面の高さに対し、外部電極8の厚さの分だけ高いところにフィルム10があるため、基板実装後のフラックスの洗浄効果があるという利点がある。また、半導体装置の中央に半導体チップ1の裏面と電気的に接続される部分がないので、基板実装時に発生するショートなどの不具合をまねかないという利点もある。なお、本実施例ではダイパッド2が存在する図で説明してきたが、実施に際しては必ずしも必要とは限らない。第3の実施例の半導体装置の作成方法を図7の断面図を用いて簡単に説明する。第3の実施例では、図7Aに示すような部分的に穴の開いたポリイミドなどのフィルム10に銅箔などの薄い導体をラミネートしてダイパッド2、内部導出リード6および外部配線11を形成し、この導体の付いたフィルム10に、前述の方法と同様に半導体チップ1を載置して電気的に接続を行い、樹脂封止および外装メッキ9を施すと図7Bにその断面を示す構造になる。さらに、加熱などを施しながら半導体装置周辺のフィルム10を剥離すると図7Cに示すような本実施例の構造となる。なお、第2の実施例と同様に外部電極8の外側の外部配線11を、フィルム10を剥離する際、切断しやすいようにあらかじめ細くしておくとよい。

【0013】さらに、第4および第5の実施例として、図8に断面図を示すように、外部電極8を2重に配置した構造も、前述してきた実施例より容易に作成される。本実施例の構造の場合、前述の実施例より半導体装置の大きさは少し大きくなるが、外部電極8同士の間隔が広くできるために基板実装時の半田によるブリッジ（電極間ショート）が発生しにくいという利点がある。

【0014】また、第6の実施例として図6の断面図に示した第3の実施例において、完成した半導体装置の中央部にあるフィルム10を除去することにより、図9に断面図に示すように、半導体チップ1の裏面部あるいは封止材5以外の樹脂材料を介した面が、外部電極8の下面よりさらに高くできるので、第3の実施例のところで述べた地盤実装時の洗浄効果がよりあがるという利点がある。

【0015】

【発明の効果】以上の説明から明らかなように、この発明の半導体装置では内部導出リードの接続点の裏面を半導体装置の外部電極としたので、半導体チップの大きさに近い寸法の半導体装置を提供できる。また、厚みに関しても、約０．５ｍｍ前後の厚みの半導体装置を提供できる。

【図面の簡単な説明】

【図１】この発明の第１の実施例の断面図。

【図２】第１の実施例の半導体装置の第１の作成方法を説明する断面図。

【図３】第１の実施例の半導体装置の第２の作成方法を説明する断面図。

【図４】この発明の第２の実施例の断面図。

【図５】第２の実施例の半導体装置の作成方法を説明する断面図。

【図６】この発明の第３の実施例の断面図。

【図７】第３の実施例の半導体装置の作成方法を説明する断面図。

【図８】この発明の第４および第５の実施例の断面図で、Ａは第４の実施例、Ｂは第５の実施例である。

【図９】この発明の第６の実施例の断面図。

【図１０】従来例の表面実装型半導体装置の断面図。

【図１１】従来例の表面実装型半導体装置を基板に実装した状態の断面図。

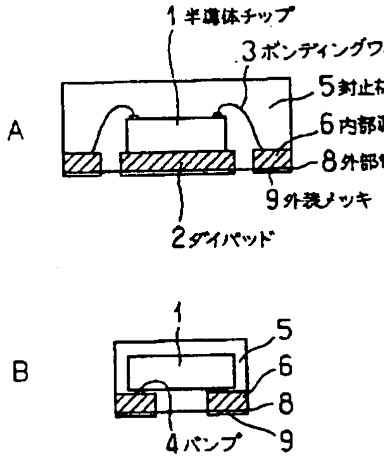
【図１２】従来例の表面実装型半導体装置の外部導出リードの変形状態を示した説明図で、Ａは斜視図、Ｂは平面図である。

【図１３】従来例の表面実装型半導体装置の断面図である。

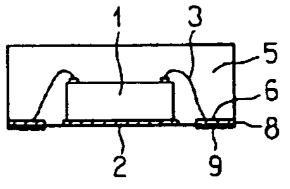
【符号の説明】

１	半導体チップ
２	ダイパッド
３	ボンディングワイヤ
４	バンプ
５	封止材
６	内部導出リード
７	外部導出リード
８	外部電極
９	外装メッキ
１０	フィルム
１１	外部配線

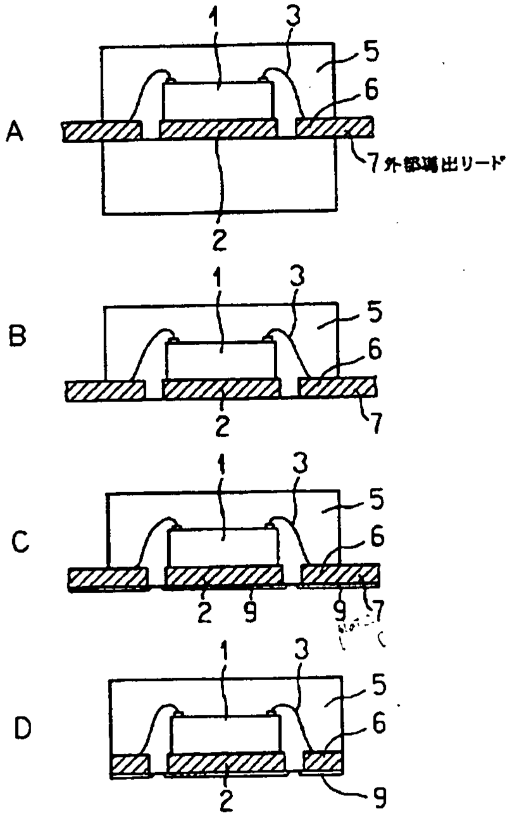
【図１】



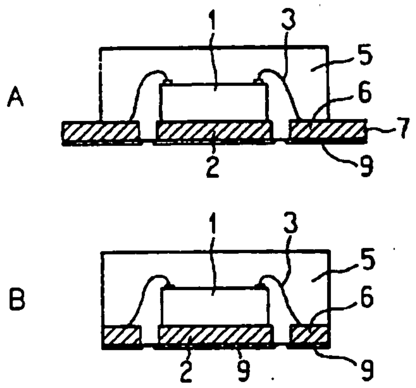
【図４】



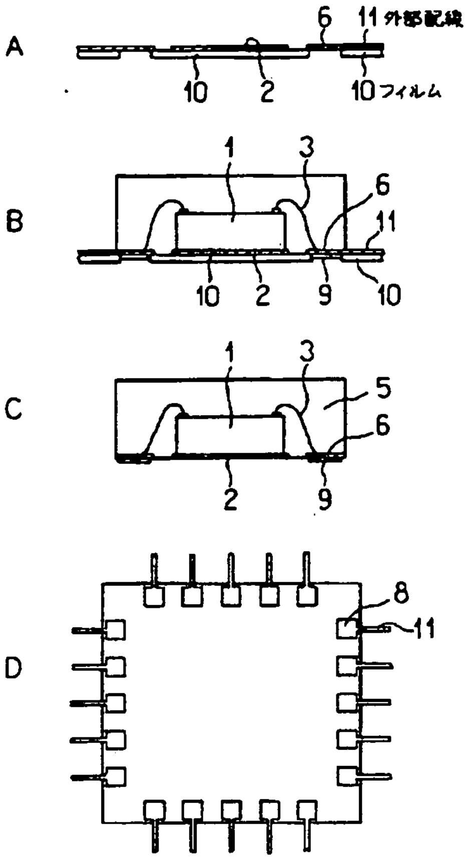
【図２】



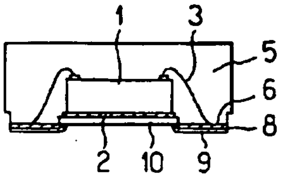
【図3】



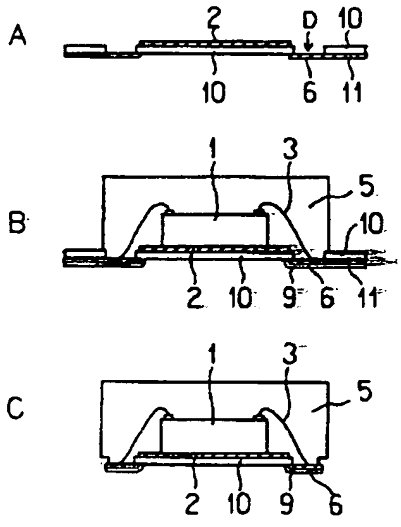
【図5】



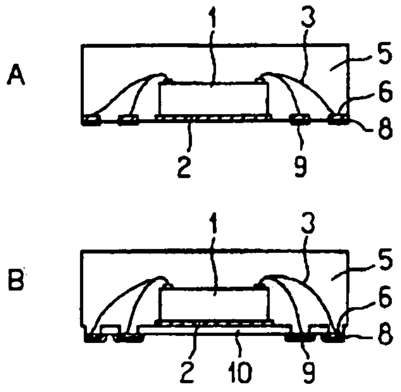
【図6】



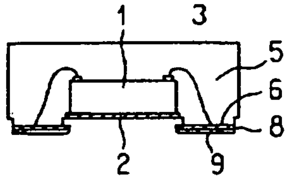
【図7】



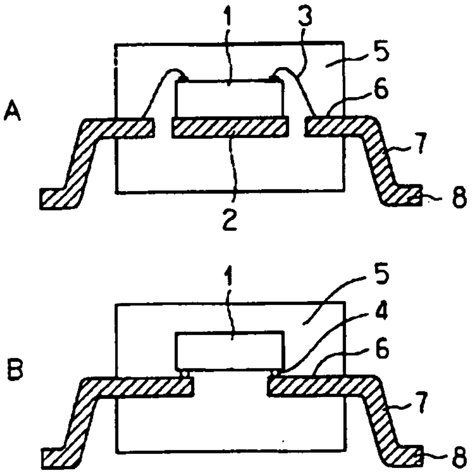
【図8】



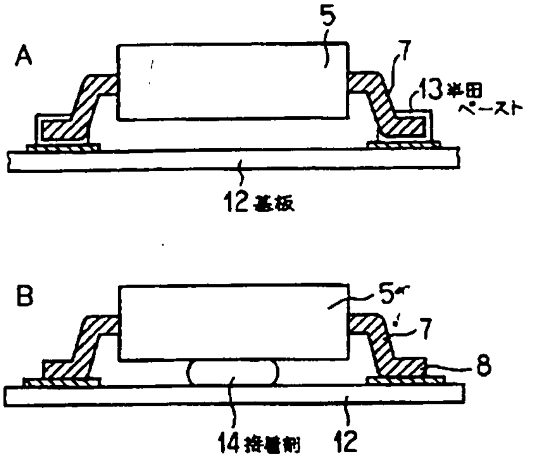
【図9】



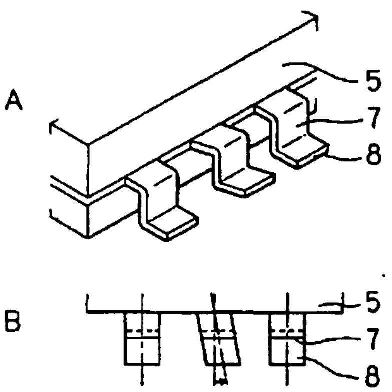
【図１０】



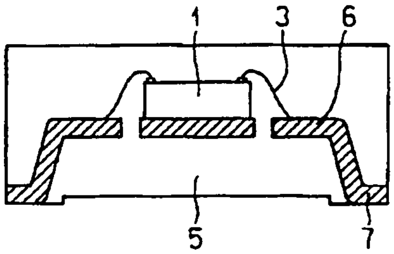
【図１１】



【図１２】



【図１３】



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		R 9272－4M		

Abstract of Japanese Patent Office Gazette

No. S60-195957

LEAD FRAME

Inventor:	Tanigawa Takahiro, et al.
Applicant:	Hitachi Ltd.
Filed:	Mar. 19, 1984
Disclosed:	Oct. 4, 1985

PURPOSE: To improve the contacting property between a lead frame and a resin and to enhance the sealability and the reliability by stepwisely forming the side of the lead frame, and increasing the contacting surface with the resin.

CONSTITUTION: Projections 8, 15 are formed on tabs 4, 13 of a lead frame, tab hanging lead 5 and the sides of leads 6, 14. The projection 8 is formed by a suitable method. The lead frame 12 is, for example, composed of 42-alloy. A semiconductor chip 9 is formed, for example, of silicon single crystal substrate, many circuit elements are formed in the chip by the know technique, and one circuit function is formed. A resin sealer 11 is formed, for example, of epoxy resin, and molded by a known transfer molding method.